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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,330	08/17/2001	Jon M. Huppenthal	SRC012	4801

25235 7590 06/28/2005

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EXAMINER	
EDELMAN, BRADLEY E	
ART UNIT	**PAPER NUMBER**
2153	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,330	HUPPENTHAL ET AL.	
	Examiner	Art Unit	
	Bradley Edelman	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) *37-51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to Applicant's amendment filed on January 25, 2005. Claims 1-36 are presented for further examination. Claims 37-51 have been withdrawn from consideration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al, 6,633,945 (Fu hereafter) in view of Scardamalia et al, 6,295,571 (Scardamalia hereafter), and further in view of Miller (5,915,104).

As per claim 1, Fu teaches a computer system comprising: at least one processor (120, fig. 2); a controller (220, fig. 2) for coupling said at least one processor to a peripheral bus control block (240, fig. 2) and a memory module bus (114, fig. 2); at least one peripheral bus slot coupled to said peripheral bus control block by a peripheral bus (151, fig. 2; PCI bus allows plurality of peripherals to be connected); at least one memory module slot coupled to said memory module bus (1300, fig. 2, col. 3, lines 41-45; memory module slots allow plurality of DIMM chips to be coupled). Fu does not explicitly disclose a processor element associated with said at least one memory

module slot for providing a data connection to an external device coupled thereto, or that the memory module slot is in direct communication with said peripheral bus.

However, in a similar art, Scardamalia discloses a memory adapter module (300, fig. 1) associated with at least one memory module slot for providing a data connection to an external device (100, fig. 1) coupled thereto (col. 5, lines 24-28). In another related art, Miller discloses a system including memory, buses, a controller, and other elements related to the Scardamalia system, and further discloses that a memory module slot could be connected directly to a peripheral bus (see Figs. 1-2, see also col. 9, describing that it is well known to have a PCI bus "directly connect[ed] to a main memory". Hence, it would have been obvious to one of ordinary skill in the art to be motivated to combine and modify the teachings of Fu, Scardamalia, and Miller to use a memory adapter module for providing data connection to external device and to allow direct communication between the memory module and the peripheral bus to increase efficiency of transactions by reducing bottlenecks and delays/latency in the memory connection fabric and the I/O channels (see Scardamalia, col. 1, lines 63-65; see also Miller, col. 9, lines 14-20).

Claim 13 is rejected for similar reasons as claim 1 above. Fu further teaches alternative embodiments of the above invention by having a controller for coupling said at least one processor to a graphics control block (240, fig. 2) and a memory module bus (114, fig. 2); at least one graphics bus connection coupled to said graphics control block by a graphics bus (154, fig. 2). at least one memory module slot coupled to said

memory module bus (1300, fig. 2, col. 3, lines 41-45; memory module slots allow plurality of DIMM chips to be coupled). Fu does not explicitly disclose a processor element associated with said at least one memory module slot for providing a data connection to an external device coupled thereto. However, Scardamalia discloses a memory adapter module (300, fig. 1) associated with at least one memory module slot for providing a data connection to an external device (100, fig. 1) coupled thereto (col. 5, lines 24-28). Hence, it would have been obvious to one of ordinary skill in the art to be motivated to combine and modify the teachings of Fu and Scardamalia to use a memory adapter module for providing data connection to external device to increase efficiency of transactions by reducing bottlenecks and delays in the memory connection fabric and the I/O channels as disclosed by Scardamalia in [col. 1, lines 63-65].

As per claims 2-4, Fu teaches a control connection to said processor element coupled to said peripheral bus for indicating to said at least one processor an arrival of data on said data connection to said processor element (see fig. 2; col. 3, lines 51-61); memory module bus comprises a DIMM bus (115, fig. 2, col. 3, line 45); processor element comprises a DIMM physical format for retention within said at least one memory module slot (col. 3, lines 45).

As per claims 5-6, in conjunction with claims 2-4, Fu teaches a DIMM memory module bus and processor element processor element comprises a DIMM physical format for retention within said at least one memory module slot as stated previously.

Fu and Scardamalia do not explicitly disclose memory module bus comprises a RIMM bus and processor element comprises a RIMM physical format for retention within said at least one memory module slot. However, it would have been obvious to one of ordinary skill in the art to introduce a variation of the Fu and Scardamalia teachings by using equivalent functional memory formats such as RIMM technologies.

As per claims 7-8, Fu teaches external device comprises one of another computer system (fig. 13; plurality of systems are interconnected to increase speed and performance); peripheral bus comprises PCI bus (153, fig. 2).

As per claims 9-10, Fu teaches the memory interface element (3108, fig. 3) is operative to alter data received from said (transaction) controller (400, fig. 3) on said memory module bus (115, fig. 3) prior to transmission on data to memory control unit (col. 5, lines 9-15). Fu does not explicitly disclose processor element (memory module) transmitting data to external device for processing. Scardamalia teaches the memory adapter module transmitting transaction requests to external device (100, fig. 1) for assistance in transactions processing (col. 5, lines 30-35). Hence, it would have been obvious to one of ordinary skill in the art to introduce a modification of the Scardamalia teachings by using external helpers (devices) to expedite transactions processing.

As per claim 11, Fu and Scardamalia do not explicitly disclose processor element comprises: a field programmable gate array configurable to perform an identified

algorithm on an operand provided thereto on said memory module bus and said data connection. However, it is well known and would have been obvious to one of ordinary skill in the art to use FPGA technology because FPGA provides an array of logic elements that are programmable and configurable based on the user's requirements.

As per claim 12, Fu teaches a system comprises a plurality of processors (120, fig. 2; CPU0, CPU1, CPU2, etc.) Fu and Scardamalia do not teach one processor comprises a plurality of processors. However, it is well known and would have been obvious to one of ordinary skill in the art to use a plurality of processors in a system to increase power and performance levels of the system.

Claims 14-16 are rejected for similar reasons as claims 2-4, 13 addressed above.

Claims 17-18 are rejected for similar reasons as claims 5-6 addressed above.

Claims 19-20 are rejected for similar reasons as claims 7-8 addressed above. Fu further teaches peripheral bus comprises an AGP bus (154, fig. 2).

Claims 21-22 are rejected for similar reasons as claims 9-10 addressed above.

Claims 23-24 are rejected for similar reasons as claims 11-12 addressed above.

Claim 25 is rejected for similar reasons as claim 1 above. Fu further teaches alternative embodiments of the above invention by having a controller for coupling said at least one processor to a graphics control block (240, fig. 2) and a memory module bus (114, fig. 2); at least one graphics bus connection coupled to said graphics control

block by a graphics bus (154, fig. 2). at least one memory module slot coupled to said memory module bus (1300, fig. 2, col. 3, lines 41-45; memory module slots allow plurality of DIMM chips to be coupled). Fu does not explicitly disclose a processor element associated with said at least one memory module slot for providing a data connection to an external device coupled thereto. However, Scardamalia discloses a memory adapter module (300, fig. 1) associated with at least one memory module slot for providing a data connection to an external device (100, fig. 1) coupled thereto (col. 5, lines 24-28). Hence, it would have been obvious to one of ordinary skill in the art to be motivated to combine and modify the teachings of Fu and Scardamalia to use a memory adapter module for providing data connection to external device to increase efficiency of transactions by reducing bottlenecks and delays in the memory connection fabric and the I/O channels as disclosed by Scardamalia in [col. 1, lines 63-65]. Furthermore, Fu and Scardamalia do not explicitly teach a controller for coupling said at least one processor to a system maintenance control block and a memory module bus; at least one system maintenance bus connection coupled to said system maintenance control block by a system maintenance bus. However, it would have been obvious to one of ordinary skill in the art to introduce various embodiments of the Fu and Scardamalia teachings such as system maintenance control block and system maintenance bus connection as a design choice without departing from the spirit and scope of the invention as disclosed by Fu in [col. 8, lines 60-63].

Claims 26-28 are rejected for similar reasons as claims 2-4 and 25 addressed above.

Claims 29-30 are rejected for similar reasons as claims 5-6 addressed above.

Claims 31-32 are rejected for similar reasons as claims 7-8 addressed above. Fu further teaches peripheral bus comprises an AGP bus (154, fig. 2). Fu and Scardamalia do not explicitly disclose peripheral bus comprises an SM bus. However, as stated in claims 13 and 25 above, it would have been obvious to one of ordinary skill in the art to include still another embodiment of the Fu teachings to include SM bus as a design choice without departing from the spirit or scope of the invention.

Claims 33-34 are rejected for similar reasons as claims 9-10 addressed above.

Claims 35-36 are rejected for similar reasons as claims 11-12 addressed above.

Response to Arguments

Applicant's arguments filed on January 25, 2005 have been fully considered but are moot in view of the new grounds for rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley Edelman whose telephone number is 571-272-3953. The examiner can normally be reached from 9 a.m. to 5 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glen Burgess can be reached at 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BE
June 23, 2005

Bradley Edelman